REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

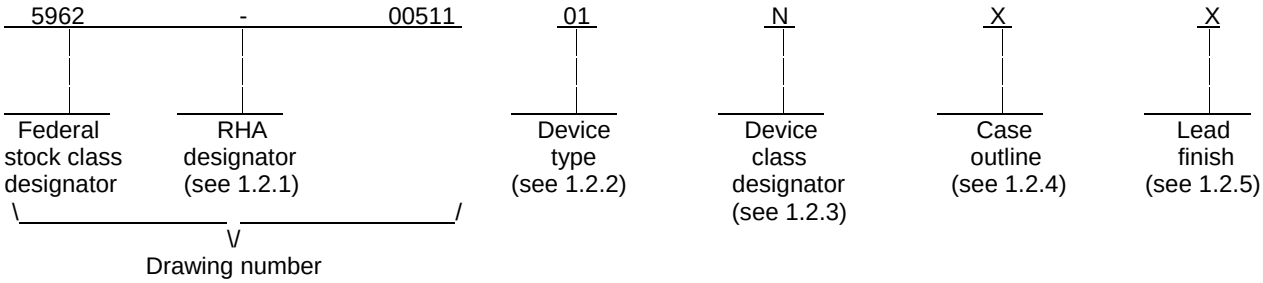
REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19															
REV STATUS				REV																
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY RAJESH PITHADIA	
	APPROVED BY RAYMOND MONNIN	MICROCIRCUIT, DIGITAL-LINEAR, 14-BIT 8 MSPS, ANALOG-TO-DIGITAL CONVERTER, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 01-01-16	
	REVISION LEVEL	SIZE: A; CAGE CODE: **67268**; **5962-00511**
		SHEET 1 OF 19

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of space application (device class V), high reliability (device classes M and Q), and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	THS1408	14-bit, 8 MSPS, analog-to-digital converter with an internal reference

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
N	Certification and qualification to MIL-PRF-38535 with a nontraditional performance environment 1/
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	48	Plastic quad flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

1/ Items which have been subjected to and passed all applicable requirements of this specification including qualification testing, screening testing, and TCI/QCI inspections, and are encapsulated in plastic.

1.3 Absolute maximum ratings. 1/

Supply voltage (AV_{DD} to AGND)	4 V
Supply voltage (DV_{DD} to DGND)	4 V
Reference input voltage range (VBG)	-0.3 V to AV_{DD} +0.3 V
Analog input voltage range	-0.3 V to AV_{DD} +0.3 V
Digital input voltage range	-0.3 V to DV_{DD} +0.3 V
Power dissipation (P_D)	360 mW
Storage temperature range	-65°C to +150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	+260°C
Thermal resistance, junction-to-case (θ_{JC})	0.79°C/W
Thermal resistance, junction-to-ambient (θ_{JA})	28.8°C/W

1.4 Recommended operating conditions.

Supply voltage range (AV_{DD}, DV_{DD})	3.0 V to 3.6 V
High level digital input (V_{IH})	2 V minimum
Low level digital input (V_{IL})	0.8 V maximum
Load capacitance (C_L)	15 pF
Clock frequency range (f_{CLK})	8 MHz
Clock duty cycle	45 % to 55 %
Output disable (t_{dis})	10 ns is a typical value
Write pulse duration high ($t_{wH(WE)}$)	15 ns minimum
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram(s). The block diagram(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figure 4.

3.2.5 Principles of operation. The principles of operation shall be as specified on figure 5.

3.3 Electrical performance characteristics and post irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply section							
Analog supply current	I_{DDA}	AV_{DD} = 3.6 V	1,2,3	01		90	mA
Digital supply current	I_{DDD}	DV_{DD} = 3.6 V	1,2,3	01		10	mA
DC characteristics section							
Differential nonlinearity	DNL		1,2,3	01		±1	LSB
Integral nonlinearity	INL		1,2,3	01		±7.5	LSB
Offset error	OE	+INPUT = -INPUT, PGA = 0 dB	1,2,3	01		0.3	%FSR
Gain error	GE	PGA = 0 dB	1,2,3	01		1.75	%FSR
AC characteristics section							
Effective number of bits	ENOB		4,5,6	01	11.2		Bits
Signal-to-noise ratio	SNR	f_{IN} = 1 MHz	4,5,6	01	70		dB
Signal-to-noise + distortion	SINAD	f_{IN} = 1 MHz	4,5,6	01	69		dB
Spurious free dynamic range	SFDR	f_{IN} = 1 MHz	4,5,6	01	71		dB
Reference voltage section							
Bandgap voltage, internal mode	VBG		1,2,3	01	1.425	1.575	V
Analog inputs section							
Positive analog input	+IN		1,2,3	01	0	AV_{DD}	V
Negative analog input	-IN		1,2,3	01	0	AV_{DD}	V
Analog input voltage difference		ΔA_{IN} = +IN - -IN, V_{REF} = +REF - -REF	1,2,3	01	$-V_{REF}$	$+V_{REF}$	V
PGA range			1,2,3	01	0	7	dB
PGA gain error			1,2,3	01		±0.25	dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital inputs section							
High level digital input	V_{IH}		1,2,3	01	2		V
Low-level digital input	V_{IL}		1,2,3	01		0.8	V
Input current	I_{IN}		1,2,3	01		±1	µA
Digital outputs section							
High-level digital output	V_{OH}	I_{OH} = 50 µA	1,2,3	01	2.6		V
Low-level digital output	V_{OL}	I_{OL} = 50 µA	1,2,3	01		0.4	V
Output current, high impedance	I_{OZ}		1,2,3	01		10	µA
Clock timing (CS low) section							
Clock frequency	fCLK		9,10,11	01		8	MHz
Output delay time	td		9,10,11	01		25	ns

1/ Unless otherwise specified, supply voltage range (AV_{DD}, DV_{DD}) will equal 3.3 V.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-PRF-38535, appendix A).

Case X

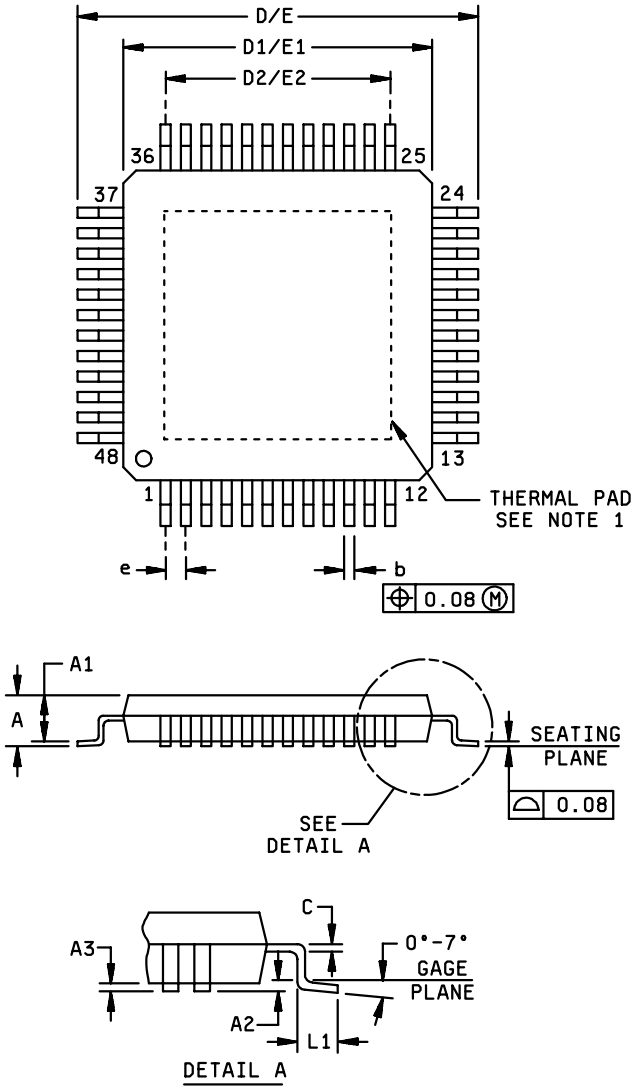


FIGURE 1. Case outline.

Case X

Symbol	Dimensions	
	Millimeters	
	Min	Max
A		1.20
A1	0.95	1.05
A2	0.25	---
A3	0.05	0.15
b	0.17	0.27
C	0.13	---
D	8.80	9.20
D1	6.80	7.20
D2	5.50	---
E	8.80	9.20
E1	6.80	7.20
E2	5.50	---
e	0.50	---
L1	0.45	0.75

NOTES:
1. The package thermal performance may be enhanced by bonding the thermal pad to an thermal plate. This pad is electrically and thermally connected to the backside of the die and possible selected leads.
2. Body dimensions do not include mold flash or protrusion.

FIGURE 1. Case outline – Continued.

Device type	01		Device type	01
Case outline	X		Case outline	X
Terminal number	Terminal symbol		Terminal number	Terminal symbol
1	-IN		25	DGND
2	AV_{DD}		26	DV_{DD}
3	VBG		27	D2
4	CML		28	D1
5	+REF		29	D0
6	-REF		30	DV_{DD}
7	AGND		31	DV_{DD}
8	AGND		32	CLK
9	DGND		33	DGND
10	OV		34	DGND
11	D13		35	$\overline{OE}$
12	D12		36	$\overline{WR}$
13	D11		37	$\overline{CS}$
14	DV_{DD}		38	NC
15	DGND		39	NC
16	D10		40	A1
17	D9		41	A0
18	D8		42	DV_{DD}
19	D7		43	AV_{DD}
20	DV_{DD}		44	AGND
21	D6		45	AGND
22	D5		46	AGND
23	D4		47	AV_{DD}
24	D3		48	+IN

NC = No connection

FIGURE 2. Terminal connections.

Terminal symbol	I/O	Description
A0; A1	I	Address input.
AGND	P	Analog ground.
AV_{DD}	P	Analog power supply.
CLK	I	Clock input.
CML		Reference midpoint. This pin requires a 0.1 μF capacitor to AGND.
$\overline{CS}$	I	Chip select input. Active low.
DGND	P	Digital ground.
DV_{DD}	P	Digital power supply.
D0 – D13	I/O	Data inputs / outputs.
NC		No connection. Do not use. Reserved.
+IN	I	Positive differential analog input.
-IN	I	Negative differential analog input.
$\overline{OE}$	I	Output enable. Active low.
OV	O	Out of range output
+REF	O	Positive reference output. This pin requires a 0.1 μF capacitor to AGND.
-REF	O	Negative reference output. This pin requires a 0.1 μF capacitor to AGND.
VBG	I	Reference input. This pin requires a 1 μF capacitor to AGND
$\overline{WR}$	I	Write signal. Active low.

FIGURE 2. Terminal connections – Continued.

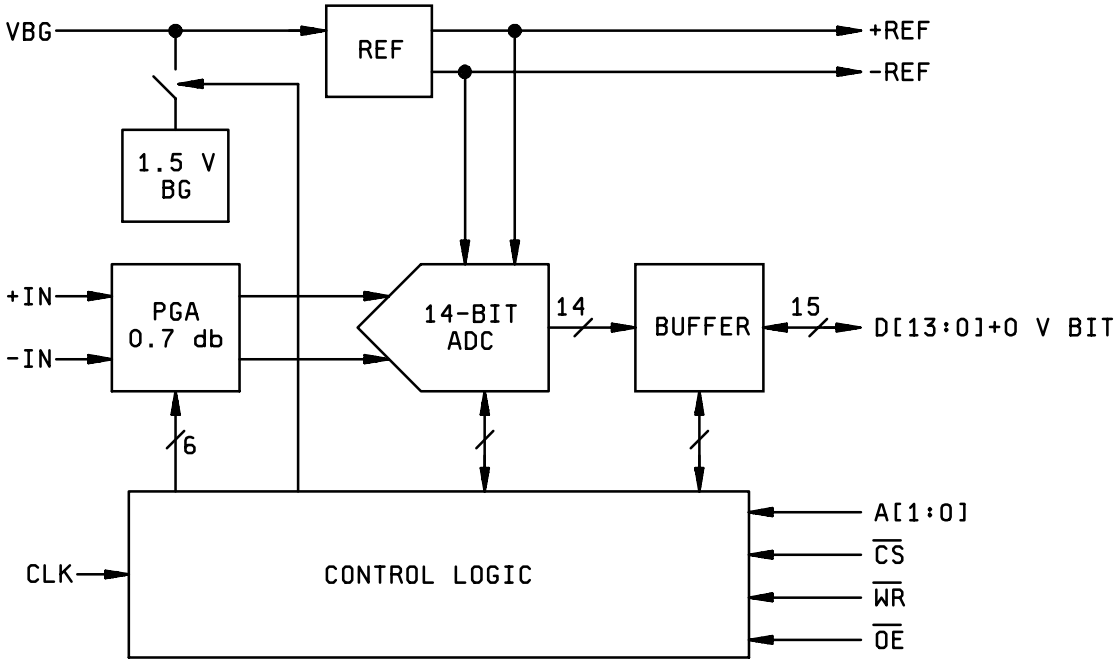
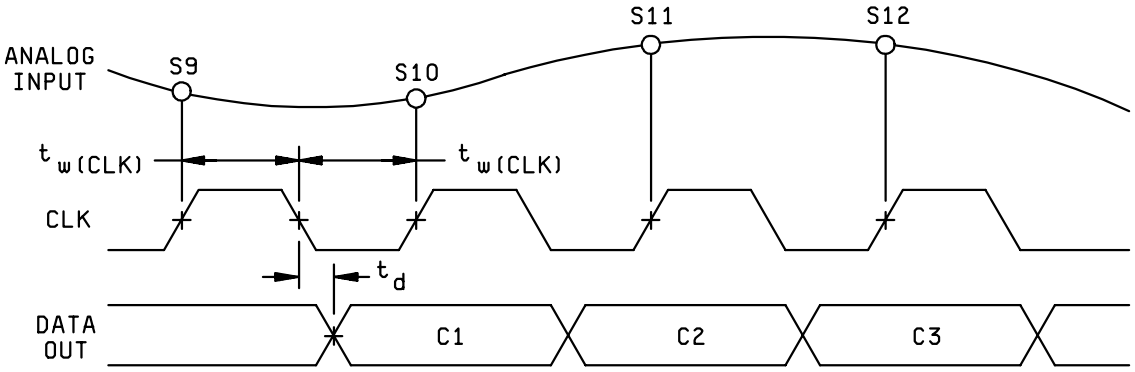


FIGURE 3. Block diagram.

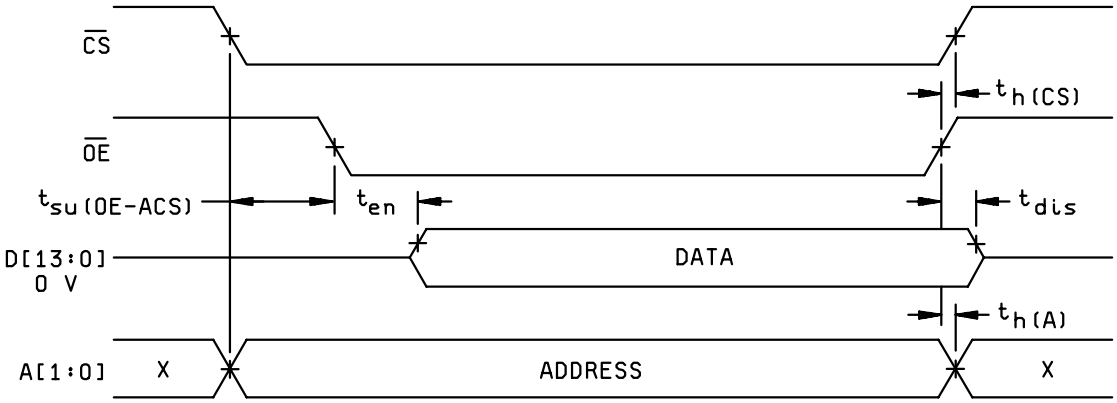
Sample timing waveform



NOTE: The device core is based on a pipeline architecture with a dormancy of 9.5 samples. The conversion results appear on the digital output of 9.5 clock cycles after the input signal was sampled. The parallel interface of the device features 3-state buffers making it possible to directly connect it to a data bus. The output buffers are enabled by driving the OE input low. Besides the sample results, it is also possible to read the values of the control register, the PGA register, and the control register. Which register is read is determined by the address inputs A1, A0. The device results are available at address 0.

FIGURE 4. Timing diagram.

Read timing waveform

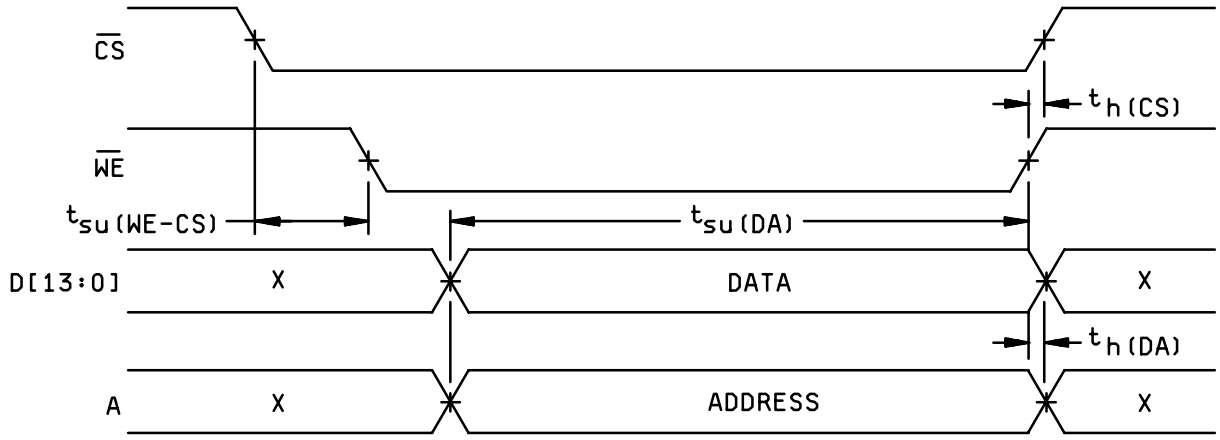


Test 1/	Symbol	Limit		Unit
		Min	Max	
Load capacitance	C_L		15	pF
Address and chip select setup time	$t_{su(OE-ACS)}$	4		ns
Output enable	t_{en}		15	ns
Address hold time	$t_{h(A)}$	1		ns
Chip select hold time	$t_{h(CS)}$	0		ns

1/ All timing tests refer to 50 % level.

FIGURE 4. Timing diagram – Continued.

Write timing waveform



Test 1/	Symbol	Limit		Unit
		Min	Max	
Load capacitance	C_L		15	pF
Chip select setup time	$t_{su(WE-CS)}$	4		ns
Data and address setup time	$t_{su(DA)}$	29		ns
Data and address hold time	$t_{h(DA)}$	0		ns
Chip select hold time	$t_{h(CS)}$	0		ns

1/ All timing tests refer to 50 % level.

FIGURE 4. Timing diagram – Continued.

Registers

The device contains several registers. The A register is selected by the values of bits A1 and A0:

A1	A0	Register
0	0	Conversion result
0	1	PGA
1	0	Offset
1	1	Control

TABLE A and B describe how to read the conversion results and how to configure the data converter. The default values (where applicable) show the state after a power-on reset.

TABLE A. Conversion result register, Address O, Read

Bit	D13	D12	D11	D10	D9	D8	D7
Function	MSB	---	---	---	---	---	---
Bit	D6	D5	D4	D3	D2	D1	D0
Function	---	---	---	---	---	---	LSB

The output can be configured for two's complement or straight binary format (see D11 / control register).

The output code is given by:

2's complement:		Straight binary:	
-8192	at ΔIN = - ΔREF	0	at ΔIN = -ΔREF
0	at ΔIN = 0	8192	at ΔIN = 0
8191	ΔIN = -ΔREF – 1LSB	16383	at ΔIN = -ΔREF – 1 LSB
1 LSB	= 2ΔREF / 16384		

TABLE B. PGA gain register, Address 1, Read / Write

Bit	D13	D12	D11	D10	D9	D8	D7
Function	X	X	X	X	X	X	X
Default	0	0	0	0	0	0	0
Bit	D6	D5	D4	D3	D2	D1	D0
Function	X	X	X	X	G2	G1	G0
Default	0	0	0	0	0	0	0

The PGA gain is determined by writing to G2-0.

Gain (dB) = 1 dB x G2-0 maximum = 7 dB. The range of G2-0 is to 0 to 7.

FIGURE 5. Principles of operation.

Registers – Continued.

TABLE C. Offset register, Address 2, Read/Write

Bit	D13	D12	D11	D10	D9	D8	D7
Function	X	X	X	X	X	X	MSB
Default	0	0	0	0	0	0	0
Bit	D6	D5	D4	D3	D2	D1	D0
Function	---	---	---	---	---	---	LSB
Default	0	0	0	0	0	0	0

NOTE: The offset correction range is from –128 to 127 LSB. This value is added to the conversion results from the device.

TABLE D. Control Register, Address 3, Read

Bit	D13	D12	D11	D10	D9	D8	D7
Function	PWD	REF	FOR	TM2	TM1	TM0	OFF
Bit	D6	D5	D4	D3	D2	D1	D0
Function	RES	RES	RES	RES	RES	RES	RES

TABLE E. Control Register, Address 3, Write

Bit	D13	D12	D11	D10	D9	D8	D7
Function	PWD	REF	FOR	TM2	TM1	TM0	OFF
Default	0	0	0	0	0	0	0
Bit	D6	D5	D4	D3	D2	D1	D0
Function	RES	RES	RES	RES	RES	RES	RES
Default	0	0	0	0	0	0	0

PWD:	Power down	0 = normal operation	1 = power down
REF:	Reference select	0 = internal reference	1 = external reference
FOR:	Output format	0 = straight binary	1 = 2's complement
TM2-0:	Test mode	000 = normal operation	
		001 = both inputs = -REF	
		010 = +IN at V_{REF} / 2, -IN at –REF	
		011 = +IN at +REF, -IN at –REF	
		100 = normal operation	
		101 = both inputs = +REF	
		110 = +IN ar –REF, -IN at V_{REF} / 2	
		111 = +IN at –REF, -IN at +REF	
OF:	Offset correction	0 = enable	1 = disable
RES	Reserved	Must be set to 0	

FIGURE 5. Principles of operation – Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---	---
Final electrical parameters (see 4.2)	1,2,3,4,5, 1/ 6,9,10,11	1,2,3,4,5, 1/ 6,9,10,11	1,2,3,4,5, 1/ 6,9,10,11	1,2,3,4,5, 1/ 6,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1	1	1	1
Group D end-point electrical parameters (see 4.4)	1	1	1	1
Group E end-point electrical parameters (see 4.4)	---	---	---	---

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-01-16

Approved sources of supply for SMD 5962-00511 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0051101NXD	01295	THS1408MPHP

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: 6412 Highway 75 South Sherman, TX 75090-9493